

SPECIFICATION

Electronic Version 1.2.8

Stylesheet Version 1.0

[DATA TRANSMISSION CIRCUIT AND METHOD]

Background of Invention

[0001] 1. Field of the Invention

[0002] The present invention relates to a data transmission circuit and method for transmitting data. More specifically, the present invention shows a data transmission circuit and method for decreasing signal interference on a data bus.

[0003] 2. Description of the Prior Art

[0004] Generally speaking, microprocessor systems processing large amounts of data with high speed all have more than one data processing unit. Some data processing units such as a memory are used to store data. Others such as a central processing unit are used to operate and process data. Moreover, data processing units are used to coordinate data exchange between other data processing units. For example, a north bridge chip on a motherboard of a computer system is used to coordinate data exchange among the central processing unit, the memory, a graphic accelerator, and a south bridge chip. To exchange data with other data processing units for completing the whole function of a microprocessor system, each data processing unit is connected via a data bus. Each data processing unit uses a data transmission circuit to electrically connect to the data bus to send or receive data on the data bus.

[0005] Please refer to Fig.1. Fig.1 is a schematic diagram of two data processing units 14 and 16 exchanging data through a data bus 12 in a typical microprocessor system 10. The microprocessor system 10 comprises two data processing units 14 and 16. Two data transmission circuits 18 and 20 are installed within the respective data processing units 14 and 16, and are electrically connected to both ends of the data

bus 12 to handle data exchanges between the data processing units 14 and 16.

[0006] Please refer to Fig.2. Fig.2 is a block diagram of a prior art data transmission circuit 22. The data transmission circuit 22 comprises an internal circuit 24, a register 28, an output circuit 32, and a control circuit 34. The internal circuit 24 is electrically connected to the register 28, the register 28 is electrically connected to the output circuit 32, and the output circuit 32 is electrically connected to the data bus 12. The control circuit 34 controls the operation of the whole data transmission circuit 22 and is electrically connected to the register 28 and the output circuit 32. The internal circuit 24 has a data output level 26 for providing data, and the register 28 has a D flip-flop 30 for temporarily storing data. A clock signal controlling the D flip-flop 30 is supplied by the control circuit 34. If data is requested to be sent on the data bus 12 from the data transmission circuit 22, the data is transmitted to the register 28 from the data output level 26 of the internal circuit 24 first. After being triggered by the clock signal, the D flip-flop 30 sequentially transmits data to the output circuit 32 from the internal circuit 24. Then, the output circuit 32 outputs the data on the data bus 12 to complete the task of the data transmission circuit 22 transmitting data to the data bus 12.

[0007] After the data is transmitted to the data bus 12, the control circuit 34 controls the output circuit 32 with a control signal to disconnect with the data bus 12 so that the data bus 12 is in a floating state. When the data bus 12 is in the floating state, the data transmission circuit 22 either waits for another data transmission circuit connected to the other end of the data bus 12 to transmit data, or readies to transmit data through the data bus 12. For all data transmission circuits electrically connected to the data bus 12, while the data bus 12 is in the floating state, a turn-around cycle can be supplied to prevent interference on the data bus 12 and prevent a phenomenon of signal contention. After the data transmission circuit finishes transmitting data, the output circuit 32 usually disconnects with the data bus for a period of time.

[0008] As mentioned above, closing the data bus 12 helps to coordinate the transmitting of data between each data transmission circuit. Nevertheless, there is still a delay period from when the control circuit 34 sends a control signal to when the output

circuit 32 totally disconnects with the data bus 12. In this delay period, the data transmission circuit 22 still transmits data to the data bus 12 through the output circuit 32. If the content of the data bus is changed (such as from high-level to low-level, or low-level to high-level) during the delay period, and then disconnected, it can be seen as an impulse signal transmitting on the data bus under the floating state. To get a more detailed understanding, please refer to Fig.3. Fig.3 is a timing diagram signals on nodes A, B, D, T, E in the data transmission circuit 22 shown in Fig.2. A horizontal axis in Fig.3 represents time. A signal 40 is a waveform of the clock signal on node T, and the control circuit 34 uses the clock signal to control the D flip-flop 30. Signal 42 represents data transmitted to the D flip-flop 30 from the data output level 26. Data packets 50, 52, 54, 56 are data that will be transmitted to the data bus 12 from the data transmission circuit 22. The D flip-flop 30 is triggered by the rising edge of the clock signal, and the data packets 50, 52, 54, 56 are transmitted to the output circuit 32 and are represented as data packets 50a, 52a, 54a, 56a in signal 44 on node B. At this time, please note that the control circuit 34 also uses a control signal 46 (on node E) to control the output circuit 32. When data packets 50a, 52a, 54a, 56a are transmitted to the output circuit 32, the signal 46 remains at a high level. Therefore, the four packets of data can be transmitted to the data bus 12, as shown on signal 48 of node D on the data bus 12. Data packets 50b, 52b, 54b, 56b in the signal 48 respectively correspond to data packets 50a, 52a, 54a, 56a in the signal 44. After transmitting the four packets of data, the control circuit 34 then changes the control signal 46 to a low-level from a high-level. In this way, the output circuit 32 disconnects with the data bus 12. Please note that the signal 42 has a follow-up data packet 58 after data packet 56. The data packet 58 is data transmitted from the data output level 26 contiguously, but the data packet 58 is not transmitted with the data packets 50, 52, 54, 56. The data packet 58 is transmitted to the output circuit 32 by the D flip-flop 30 when triggered by the clock signal. This is the case with data packet 58a in the signal 44. If the control signal 46 is immediately pulled low at the point of 60, the data packet 58a will still be transmitted to the data bus 12 because of the delay period, as shown with the data packet 58b in the signal 48. In the delay period, the data bus 12 still receives a small piece of data packet 58b from the output circuit 32, as the marked area 62 in the signal 48. In the delay period time, if contents of the data packet 56b and the data packet 58b are different, the

signal level on the data bus 12 will be changed. However, the signal level is not changed to a stable state and the data bus 12 has been totally disconnected so that the signal 48 in the area 62 is an impulse signal. Since the data bus 12 is disconnected and in a floating state, two ends of the data bus 12 are equivalent to an open state. The impulse signal will be reflected by both ends of the route and will be transmitted back and forth on the data bus 12 continuously. Once the data bus 12 reconnects to transmit data, the impulse signal will interfere with the normal data transmission on the data bus 12, and then the operation of the whole microprocessor system is affected.

[0009] To solve the problem of the impulse signal, one solution of the prior art method is to disconnect the data bus 12 earlier. Please refer to Fig.4 of a timing diagram of each node. The legend of Fig.4 is the same as that of Fig.3. Signals 64, 66, 68, 70, 72 are respective signals on nodes T, A, B, E, D in the data transmission circuit in Fig.2. Data packets 74, 76, 78, 80 in the signal 66 are four pieces of data that are transmitted to the data bus 12. To prevent generation of the impulse signal, the control circuit 34 controls the output circuit 32 to disconnect the data bus 12 by pulling the control signal low at the point of 82. Because the data packet 80a in the signal 68 (on node B) has not completed a cycle, this ensures that the data packet 84a following the data packet 80a is not transmitted to the data bus. However, this shortens the cycle of the data packet 80a.

[0010] Another prior art method to prevent the impulse signal is described with Fig.5. Please refer to Fig.5 of a timing diagram of each node signal in another prior art method of preventing generation of the impulse signal. The legend of Fig.5 is the same as those of Fig.3 and Fig.4. The horizontal axis is time, and signals 85, 86, 88, 90, 92 are respective signals on nodes T, A, B, E, D in Fig.2. Data packets 94, 96, 98, 100 in the signal 86 are transmitted. In the prior art method, the control circuit 34 delays the time for sending the control signal 90 at the point of 102. After the last data packet 100a of the signal 88 (on node B) is transmitted, more than half the cycle time of the signal 85 is spent waiting. Then the control signal 102 controls the control circuit 32 to disconnect the data bus 12. This way allows data packet 104a to reach a stable state in a half cycle of the signal 85 and disconnect the data bus 12 to prevent the impulse signal from being generated. Since the data packet 104b in the signal 92

will not be transmitted, the prior art method will not affect the four packets of data (i.e. data packets 94b, 96b, 98b, 100b in the signal 92) and avoids generating the impulse signal. The key to the prior art method is that the data packet 104a reaches a stable state in the half cycle of the signal 85. If the data packet 104a cannot reach a stable state in the half cycle of the signal 85, the generation of impulse signal cannot be prevented. By improving the art, the operating frequency of each data processing unit in the microprocessor system 10 increases, and the cycle of the signal 85 becomes very short. Therefore, in high-speed microprocessor systems, the data 104a cannot reach a stable state in the half cycle of the signal 85, and the impulse signal is still generated.

Summary of Invention

- [0011] It is therefore a primary objective of the claimed invention to provide a data transmission circuit to solve the above-mentioned problems.
- [0012] According to the claimed invention, the data transmission circuit comprises an internal circuit for providing data, a register electrically connected to the internal circuit for temporarily storing the data transmitted from the internal circuit, and a control circuit for controlling operation of the data transmission circuit. If data inputted to the register is a specific data, the internal circuit will repeatedly output the specific data to the register so as to prolong transmission time of the specific data.
- [0013] It is an advantage of the claimed invention that the data transmission circuit can prevent the impulse signal signals from being generated even on a high-speed data bus.
- [0014] These and other objectives and advantages of the claimed invention will no doubt become obvious to those of ordinary skill in the art after having read the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of Drawings

- [0015] Fig.1 is a diagram of two data processing units exchanging data with a data bus in a microprocessor system.

- [0016] Fig.2 is a block diagram of a prior art data transmission circuit.
- [0017] Fig.3 is a timing diagram of each signal on nodes when the prior art data transmission circuit shown in Fig.2 operates.
- [0018] Fig.4 is a timing diagram of each node signal when the prior art data transmission circuit shown in Fig.2 operates with a second method.
- [0019] Fig.5 is a timing diagram of each node signal when the prior art data transmission circuit shown in Fig.2 operates with a third method.
- [0020] Fig.6 is a block diagram of the present invention data transmission circuit.
- [0021] Fig.7 is a timing diagram of each signal on nodes when the data transmission circuit shown in Fig.6 operates.

Detailed Description

- [0022] Please refer to Fig.6 of a block diagram of the present invention data transmission circuit 110. The data transmission circuit 110 comprises an internal circuit 120, a register 130, an output circuit 140, and a control circuit 150. The internal circuit 120 has a data output level 122 and a multiplexer 124. The multiplexer 124 has a first input end 126, a second input end 128, and a selecting end 129. The second input end 128 is electrically connected to the data output level 122, and the selecting end 129 is electrically connected to the control circuit 150. The register 130 has a D flip-flop 132. An input end of the D flip-flop 132 is electrically connected to an output end of the multiplexer 124 and an output end of the D flip-flop 132 is electrically connected to the output circuit 140. The output end of the D flip-flop 132 also has a feedback route electrically connected to the first input end 126 of the multiplexer 124. The output circuit 140 is electrically connected to a data bus 108 to transmit data to the data bus 108. The control circuit 150 is electrically connected to the selecting end 129 of the multiplexer 124, the D flip-flop 132, and the output circuit 140, to control the operations of these function blocks. The control circuit 150 uses a selecting signal to control the multiplexer 124 so that the multiplexer 124 outputs the signal inputted from the first input end 126 or the second input end 128.

- [0023] The operation and principle for preventing the impulse signal of the present

invention data transmission circuit 110 is described in the timing diagram of Fig.7. Please refer to Fig.7 of a timing diagram of each signal on nodes of the data transmission circuit 110 shown in Fig.6. The horizontal axis of Fig.7 is time. Signals 160, 162, 164, 166, 168, 170, 172 are respective signals on node T1, the second input end 128, the first input end 126, the selecting end 129, node A1, node E1, and node D1. When the data transmission circuit 110 operates, the control circuit 150 controls the operation of the D flip-flop with the clock signal 160. Data to be transmitted is inputted to the second input end 128 of the multiplexer 124 from the data output level 122 first. Data packets 180, 182, 184, and 186 in the signal 162 on the second input end 128 are four packets of data to be transmitted to the data bus 108. The data packet 186 is the last packet to be transmitted.

[0024]

When data packet 180 is transmitted to the second input end 128 from the data output level 122, the control circuit 150 inputs the high-level signal of the selecting signal 166 into the selecting end 129 of the multiplexer 124. The high-level signal makes the multiplexer 124 output the signal inputted from the second input end 128. Hence, the signal inputted to the second input end 128 from the data output level 122 is outputted to the D flip-flop 132, as with the signal 168 on node A1. When the selecting signal 166 is in a high state, the signal 168 outputted to the D flip-flop by the multiplexer 124 is the signal 162 inputted from the second input end 128. The data packets 180, 182, 184 in the signal 162 become respective data packets 180b, 182b, 184b in the signal 168. After the data is transmitted to the D flip-flop 132, the D flip-flop 132 transmits the data to the output circuit 140 according to the rising edge of the clock signal 160 sent from the control circuit 150. Please note that in the present invention data transmission circuit 110, the output end of the D flip-flop 132 is not only electrically connected to the output circuit 140, but also electrically connected to the first input end 126 of the multiplexer 124. In this way, the signal 164 on the first input end 126 is also the signal transmitted to the output circuit 140 from the D flip-flop 132. The data packets 180a, 182a, 184a in the signal 164 are respective data outputted by the D flip-flop 132. At this time, the selecting signal 166 used to control the multiplexer 124 in the control circuit 150 remains at a high level, so the signal 168 outputted by the multiplexer 124 is from the second input end and has no relationship with the first input end 126. When the data packet 180a in the

signal 164 starts to be transmitted to the output circuit 140, the control circuit 150 controls the output circuit 140 to connect with the data bus 108 through a high-level in the control signal 170 on the node E1. Therefore, the signal 164 can be transmitted to the data bus 108 from the output circuit 140, shown as the signal 172 of the node D1 on the data bus 108. The data packets 180c, 182c, 184c in the signal 172 become the data packets 180a, 182a, 184a in the signal 164, respectively.

[0025] When the last data packet 186 starts to transmit to the multiplexer 124, the control circuit 150 still controls the multiplexer 124 to choose the signal inputted from the second input end 128. The last data packet 186 in the signal 162 becomes the data packet 186b in the signal 168 after being outputted by the multiplexer 124.

[0026] At time t1, the data packet 186b in the signal 168 is transmitted to the output circuit 140 (please refer to the horizontal axis in Fig.7), and at the same time, it feeds back to the first end 126 of the multiplexer 124, shown by the data packet 186a in the signal 164. The data packet 186a in the signal 164 is the same as the data packet 186c in the signal 172 during the period between t1 and t2.

[0027] At time t2, the control circuit 150 controls the multiplexer 124 by using the selecting signal 166 with a low-level at the point of 190 so that the multiplexer 124 outputs the signal 164 of the first input end 126. During the low level period of the selecting signal 166, the content of the signal 164 is simply the content of the data packet 186a. The content of the data packet 186a is outputted by the multiplexer 124 and becomes data packet 194 in the signal 168 on node A1. Please note that the content of the data packet 194 is completely the same as the content of the last data packet 186. After being triggered by the rising edge of the clock signal 160 at time t3, the D flip-flop 132 will transmit the data packet 194 in the signal 168 to the output circuit 140, shown by the data packet 196 in the signal 164. The data packet 196 in the signal 164 becomes the data packet 198 in the signal 172 of the node D1 on the data bus through the output circuit 140. After time t3, all the four data packets are transmitted to the data bus 108. Additionally, the content of the last data packet 186 will repeat in the data 198 on the signal 172. Likewise, the transmission time on the data bus 108 of the last data packet 186 is extended (originally, the transmission time of each data packet is equal to a timing cycle of the clock signal 160). After time t3,

the control circuit 150 can use the low-level control signal 192 in the signal 170 to control the output circuit 140 to disconnect the data bus 108 at any time, and is not affected by the impulse signal on the data bus.

[0028] By extending the transmission time of the last data packet 186, the present invention data transmission circuit 110 can avoid generating the impulse signal on the data bus. In the prior art, the impulse signal is generated during the period between the data bus starting to disconnect and being totally disconnected. The present invention data transmission circuit can extend the transmission time of the last data packet 186 and disconnect with the data bus during the extending transmission time. Even if the time needed by the data bus to be totally disconnected is longer, the content of the data will not be changed during the time of disconnecting the data bus. Therefore, the present invention data transmission circuit 110 can avoid producing impulse signals on the data bus and ensure that each data processing unit of the whole microprocessor system exchanges data smoothly and correctly.

[0029] The spirit of the present invention data transmission circuit is to extend the transmission time of the last data packet to be transmitted. In this way, the content of the data on the data bus is identical during the time when the data bus starts to be disconnected to being totally disconnected to prevent generation of impulse signals on the data bus. In the actual circuit, the present invention data transmission circuit uses a multiplexer to control a feedback route to achieve the objective of extending the transmission time of the specific data and reducing the noise interference on the data bus. One of the advantages of the present invention is suitability for transmitting high-speed data. For example, the present invention could be used in the north bridge chips used to control data transmission between the CPU (Central Processing Unit with memory such as RAM (Random Access Memory) on the motherboard in normal computers.

[0030] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.